WE CLAIM:

1. A method for depositing a thin film, comprising:

introducing a gas comprising trisilane to a chamber, wherein the chamber contains a substrate having a substrate surface roughness;

establishing trisilane chemical vapor deposition conditions in the chamber; and

depositing a Si-containing film onto the substrate, the Si-containing film having a thickness in the range of 10 Å to 150 Å and a film surface roughness that is greater than the substrate surface roughness by an amount of about 5 Å rms or less, over a surface area of about one square micron or greater.

2. The method of Claim 1, wherein the Si-containing film is deposited as an amorphous film.

3. The method of Claim 1, wherein the Si-containing film is deposited as an epitaxial film.

4. The method of Claim 1, wherein the Si-containing film is deposited as a polycrystalline film.

5. The method of Claim 2, wherein the Si-containing film is deposited directly onto a non-single crystal material.

6. The method of Claim 2, wherein the Si-containing film is deposited directly onto a dielectric material.

7. The method of Claim 6, wherein the dielectric material is selected from the group consisting of silicon oxide, metal oxide, metal silicate, silicon oxynitride and silicon nitride.

8. The method of Claim 6, wherein the film surface roughness is about 3 Å rms or less.

9. The method of Claim 2, further comprising depositing an oxide layer directly onto the Si-containing film.

10. The method of Claim 9, further comprising annealing the Si-containing film to form a plurality of quantum dots.

11. The method of Claim 6, further comprising depositing a doped Si-containing layer directly onto the Si-containing film.

12. The method of Claim 11, wherein the doped Si-containing layer further comprises germanium.

13. The method of Claim 12, wherein the doped Si-containing layer further comprises carbon.

14. The method of Claim 2, wherein the Si-containing film has a thickness non-uniformity of about 10% or less for a mean film thickness in the range of 100 Å to 150 Å, a thickness non-uniformity of about 15% or less for a mean film thickness in the range of 50 Å to 99 Å, and a thickness non-uniformity of about 20% or less for a mean film thickness of less than 50 Å.

15. The method of Claim 2, wherein the substrate comprises a step or trench.

16. The method of Claim 15, further comprising annealing the amorphous Si-containing film to form hemispherical grained silicon.

17. The method of Claim 2, wherein the gas further comprises a dopant element selected from the group consisting of boron, arsenic, antimony, indium, and phosphorous.

18. The method of Claim 17, wherein the Si-containing film is a diffusion layer.

19. The method of Claim 17, wherein the depositing of the Si-containing film onto the substrate results in uniform incorporation of the dopant element throughout the Si-containing film.

20. The method of Claim 2, wherein establishing trisilane chemical vapor deposition conditions comprises heating the substrate to a temperature in the range of about 400°C to about 750°C in the absence of a plasma.

21. The method of Claim 1, wherein establishing trisilane chemical vapor deposition conditions comprises heating the substrate to a temperature in the range of about 450°C to about 650°C in the absence of a plasma.

22. The method of Claim 1, wherein the Si-containing film is a Si-N film.

23. The method of Claim 22, wherein the gas further comprises a nitrogen precursor.

24. The method of Claim 23, wherein the nitrogen precursor is atomic nitrogen.

25. The method of Claim 23, wherein the Si-containing film has a hydrogen content that is less than about 4 atomic %.

26. The method of Claim 1, wherein establishing trisilane deposition conditions comprises maintaining a chamber pressure between about 1 Torr and 100 Torr.

27. A method for depositing a thin film, comprising:

introducing trisilane to a chamber, wherein the chamber contains a substrate; and

depositing a continuous amorphous Si-containing film having a thickness of less than about 100 Å and a surface area of about one square micron or larger onto the substrate by thermal chemical vapor deposition.

28. The method of Claim 27, wherein the substrate comprises a non-single crystal material.

29. The method of Claim 28, wherein the Si-containing film is deposited directly onto the non-single crystal layer and the non-single crystal layer is selected from the group consisting of silicon oxide, metal oxide, metal silicate, silicon oxynitride and silicon nitride.

30. The method of Claim 27, wherein the Si-containing film has a surface roughness of about 5 Å or less.

31. The method of Claim 27, wherein the substrate comprises a step or trench.

32. The method of Claim 31, wherein the Si-containing film has a thickness non-uniformity of about 15% or less for a mean film thickness in the range of 50 Å to 99 Å, and a thickness non-uniformity of about 20% or less for a mean film thickness of less than 50 Å.

33. The method of Claim 27, wherein the depositing is conducted at a temperature in the range of about 450°C to about 650°C.

34. The method of Claim 27, wherein the depositing is conducted in or near a mass transport limited regime for trisilane.

35. The method of Claim 34, wherein the continuous amorphous Si-containing film has a surface area of about five square microns or larger.

36. The method of Claim 27, further comprising depositing an oxide layer over the Si-containing film.

37. The method of Claim 36, further comprising annealing the Si-containing film to form a plurality of quantum dots.

38. The method of Claim 27, further comprising depositing a doped Si-containing layer directly onto the Si-containing film.

39. The method of Claim 38, wherein the doped Si-containing layer further comprises germanium.

40. The method of Claim 39, wherein the doped Si-containing layer further comprises carbon.

41. The method of Claim 27, further comprising annealing the amorphous Si-containing film to form hemispherical grained silicon.

42. The method of Claim 27, wherein the depositing is conducted at a temperature in the range of about 425°C to about 700°C.

43. The method of Claim 27, further comprising introducing a nitrogen precursor to the chamber.

44. The method of Claim 43, wherein the trisilane is introduced to the chamber in one or more pulses.

45. The method of Claim 44, wherein the nitrogen precursor is atomic nitrogen.

46. The method of Claim 45, wherein the depositing is conducted at a temperature in the range of about 450°C to about 650°C.

47. A method of increasing semiconductor manufacturing device yield, comprising:

identifying a semiconductor device manufacturing process that comprises depositing a Si-containing film onto a substrate using silane to produce a number N_T of semiconductor devices, of which a number N_A of the devices are acceptable and a number N_U of the devices are unacceptable; wherein the Si-containing film has an average thickness of about 2000 Å or less; wherein the substrate has a surface area of about 300 cm^2 or greater; and wherein the process has a device yield equal to N_A/N_T; and

replacing the silane with trisilane in the semiconductor device manufacturing process to increase the device yield.

sub A3

48. The method of Claim 47, wherein the semiconductor device manufacturing process comprises thermal CVD of silane at a temperature T_s, further comprising depositing the trisilane by thermal CVD at a temperature T_t, where $T_s > T_t$.

49. The method of Claim 47, wherein the semiconductor device manufacturing process comprises introducing trisilane to a chamber, further comprising using a bubbler to introduce the trisilane to the chamber.

50. The method of Claim 49, wherein the bubbler is temperature-regulated.

51. An integrated circuit comprising a continuous amorphous Si-containing film having a thickness that is 15 Å or greater and that is 150 Å or less, a surface area of about one square micron or greater, and a thickness non-uniformity of about 10% or less for a mean film thickness in the range of 100 Å to 150 Å, a thickness non-uniformity of about 15% or less for a mean film thickness in the range of 50 Å to 99 Å, and a thickness non-uniformity of about 20% or less for a mean film thickness of less than 50 Å

52. The integrated circuit of Claim 51, further comprising a dielectric material having a surface in contact with the Si-containing film, wherein the surface in contact has an area of about 0.5 square micron or greater.

53. The integrated circuit of Claim 51, wherein the Si-containing film further comprises a dopant element selected from the group consisting of boron, arsenic, and phosphorous.

54. The integrated circuit of Claim 53, wherein the dopant element is uniformly distributed throughout the Si-containing film.